Hall Ticket Number:

Code No. : 14448 AS

VASAVI COLLEGE OF ENGINEERING *(AUTONOMOUS)*, HYDERABAD

Accredited by NAAC with A++ Grade

B.E. (E.C.E.) IV-Semester Advanced Supplementary Examinations, September-2022.

Computer Organization and Architecture

Time: **3 hours** Max. Marks: **60**

*Note: Answer all questions from **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

Q. No.	Stem of the question	M	L	CO	PO
1.	Differentiate between 2nd and 3rd Computer generations?	2	2	1	1
2.	Represent the number (+46.5), as a floating-point binary number with 24 bits. The normalized fraction mantissa has 16 bits and the exponent has 8 bits.	2	2	1	1
3.	List any four Architectural features of 8085µp?	2	1	2	2
4.	List the Capabilities of a micro program sequencer?	2	1	2	2
5.	State Amdahl's Law and write the expression for evaluating speed up of a Processor?	2	1	3	1
6.	Define data Hazard and suggest any two methods to avoid data hazard in pipelining?	2	3	3	1
7.	Write the factors to be considered in designing the I/O interface circuit?	2	2	4	2
8.	Draw the schematic diagram for Daisy chain Interrupt method?	2	1	4	1
9.	If a system has a memory capacity of 1MB and it is partitioned into 8 segments what is the size of each segment?	2	3	5	1
10.	Define Hit ratio and how does it affect the performance of the CPU?	2	2	5	1
	Part-B (5×8 = 40 Marks)				
11. a)	Perform the multiplication of (+9) and (-13) using Booth's multiplication algorithm?	5	3	1	1
b)	Distinguish between Fixed point and Floating point representation of a given number with a suitable example?	3	2	1	1
12. a)	Define Interrupt? Write a brief note on Interrupts of 8085µp?	4	2	2	2
b)	Explain the various Registers of 8085µp?	4	1	2	2
13. a)	Define CISC and RISC and compare any four features of CISC and RISC?	4	3	3	2
b)	Explain the working of Arithmetic pipeline with a suitable example?	4	2	3	1

Contd... 2

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14. a)	Explain the operation of a Parallel Priority encoder with a suitable diagram?	4	2	4	1
b)	Explain source initiated asynchronous data transfer procedure with necessary diagram?	4	2	4	1
15. a)	Explain the concept of Associative memory with a neat block diagram?	4	2	5	1
b)	Explain the Direct mapping method of Cache organization with a suitable diagram?	4	3	5	2
16. a)	Explain an algorithm for adding and subtracting of Fixed point numbers?	4	2	1	1
b)	Explain the working of a Hardwired Control unit with a suitable diagram?	4	1	2	1
17.	Answer any ***two*** of the following:				
a)	Draw the Space time diagram for a 4-stage Instruction pipeline executing 6 instructions with stages as FI-Fetch DI-Decode EX-Execute and MWR-Memory Write?	4	3	3	1
b)	Draw the flow diagram explaining CPU-IOP Communication?	4	2	4	1
c)	Explain the virtual memory address translation with necessary diagram?	4	3	5	1

M : Marks; L: Bloom's Taxonomy Level; CO; Course Outcome; PO: Programme Outcome

i)	Blooms Taxonomy Level – 1	20%
ii)	Blooms Taxonomy Level – 2	40%
iii)	Blooms Taxonomy Level – 3 & 4	40%

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